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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **07 /08 /2023** | **Batch No:** | **C2** |
| **Faculty Name:** |  | **Roll No:** | **16010122267** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 3**

**Title: 4:1 Multiplexer and 3: 8 Decoder**

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| **Aim and Objective of the Experiment:** |
| To design and implement a 4:1 multiplexer and 3: 8 Decoder |

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| **COs to be achieved:** |
| **CO2**: Use different minimization technique and solve combinational circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Multiplexer:** Multiplexer is a special type of combinational circuit. It is a digital circuit that selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select lines. To select n inputs we require m select lines, such that 2m=n. Depending on the digital code applied at the select inputs, one out of the n data sources is selected and transmitted to a single output.  **Decoder:** A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to-one mapping from input code words into output code words. The general structure of a decoder circuit is shown in the Figure below. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. The most commonly used input code is an N-bit binary code, where an N-bit word represents one of 2N different coded values. Normally, they range from 0 through 2N − 1. The input code lines select which output is active. The remaining output lines are disabled.  **Implementation Details:**  **4:1 Multiplexer Block Diagram**    **4:1 Multiplexer Circuit**  Digital Circuits - Multiplexers | Tutorialspoint  **Pin Diagram IC74153**    **Implementation Details of 8:1 MUX**  An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input  select lines S0 through S2 and a single output line Y. Depending on the select  lines combinations, multiplexer selects the inputs*.*  **Circuit Diagram of 8:1 MUX**                    **Truth Table for 8:1 Multiplexer**                        **From Truth Table:**      **Pin diagram: IC 74151** |

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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 74153 and place the IC on trainer kit. 2. Connect VCC and ground to respective pins of IC trainer kit. 3. Implement the circuit as shown in the circuit diagram. 4. Connect the inputs to the input switches provided in the trainer kit. 5. Connect the outputs to the switches of O/P LEDs 6. Apply various combinations of inputs according to the truth table and observe the condition of LEDs. 7. Note down the corresponding output readings for various combinations of inputs. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. Design and verify a 2:1 multiplexer using logic gates. 2. Build an 8:1 multiplexer using only 2:1 multiplexers.   Ans1:        Ans2: |

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| **Conclusion:** |
| We successfully implemented 4:1 multiplexer and 3:8 Decoder. |

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| **Signature of faculty in-charge with Date:** |